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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/803,265	03/09/2001	Yoshitaka Tsunashima	790001-2002	7077

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EXAMINER	
DOLAN, JENNIFER M	
ART UNIT	PAPER NUMBER
2813	5

DATE MAILED: 11/18/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/803,265	TSUNASHIMA ET AL.
	Examiner	Art Unit
	Jennifer M. Dolan	2813

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *8/30/02* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *6-11 and 14-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5, 12, 13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Group II, claims 1-5, 12, and 13, in Paper No. 4, filed 8/30/02, is acknowledged.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

3. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No 6,020,243 to Wallace et al.

Wallace discloses a semiconductor device (figure 1; column 1, lines 15-44) comprising: a gate insulating film (column 2, lines 28-30) at least part of which includes an insulating film containing metal, silicon, and oxygen (column 2, lines 28-30; lines 45-58); wherein nitrogen is contained in the insulating film containing metal, silicon, and oxygen (column 2, lines 28-58).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 2 and 5 are rejected under 35 U.S.C. 102(e) as anticipated by U.S. Patent No. 6,057,584 to Gardner et al., or, in the alternative, under 35 U.S.C. 103(a) as obvious over Gardner et al. in view of Wallace et al.

Regarding claim 2, Gardner discloses a semiconductor device (column 1, lines 21-38) comprising: a semiconductor substrate (202; column 4, lines 3-8); a gate insulating film (204,206, and 208; column 3, lines 57-64) provided on the semiconductor substrate (figure 2f), at least part of the gate insulating film containing a metal oxide film (208, column 5, lines 3-18). Insofar as the applicant defines the insulating film containing metal, silicon, and oxygen as a film which may contain separated metal oxide and silicon oxide (see page 7 of the specification of the present application, lines 10-17), Gardner is considered to include an insulating film (204 and 206) containing metal, silicon, and oxygen (column 4, lines 15-54), provided between the semiconductor substrate and the metal oxide film (figure 2f), and nitrogen contained in the insulating film containing metal, silicon, and oxygen (column 4, lines 15-25).

Alternatively, assuming arguendo, the silicon oxynitride/metal oxide laminate of Gardner cannot be considered an insulating film containing metal, silicon, and oxygen.

Wallace discloses a single, graded composition gate insulating film containing metal, silicon, and oxygen (column 2, lines 28-30; lines 45-58).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the silicon oxynitride/metal oxide laminated films of Gardner such that they comprise a single insulating film, as taught by Wallace. The rationale is as follows: One of ordinary skill in the art at the time the invention was made would have been motivated to replace the laminate film with a single, graded film, because the structure of the graded film is substantially similar to the laminate film (Wallace, column 6, lines 43-54), but provides the additional benefit of reduced interface state densities due to bonding of discontinuous materials (Wallace, column 2, lines 46-61).

Regarding claim 5, Gardner discloses a semiconductor device (column 1, lines 21-38) comprising: a semiconductor substrate (202; column 4, lines 3-8); a gate insulating film (204,206, and 208; column 3, lines 57-64) provided on the semiconductor substrate (figure 2f), at least part of the gate insulating film containing a metal oxide film (208, column 5, lines 3-18). Insofar as the applicant defines the insulating film containing metal, silicon, and oxygen as a film which may contain separated metal oxide and silicon oxide (see page 7 of the specification of the present application, lines 10-17), Gardner is considered to include an insulating laminate film (204 and 206) containing metal, silicon, and oxygen (column 4, lines 15-54), provided between the semiconductor substrate and the metal oxide film (figure 2f), wherein a main metal element constituting the metal oxide film (column 5, lines 3-18) and a main metal element constituting the insulating film (column 4, lines 44-54) are different from each other.

Alternatively, assuming arguendo, the silicon oxynitride/metal oxide laminate films of Gardner cannot be considered an insulating film containing metal, silicon, and oxygen.

Wallace discloses a single, graded composition gate insulating film containing metal, silicon, and oxygen (column 2, lines 28-30; lines 45-58).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the silicon oxynitride/metal oxide laminated films of Gardner such that they comprise a single insulating film, as taught by Wallace. The rationale is as follows: One of ordinary skill in the art at the time the invention was made would have been motivated to replace the laminate film with a single, graded film, because the structure of the graded film is substantially similar to the laminate film (Wallace, column 6, lines 43-54), but provides the additional benefit of reduced interface state densities due to bonding of discontinuous materials (Wallace, column 2, lines 46-61).

6. Claims 3 and 4 are rejected under 35 U.S.C. 102(e) as anticipated by U.S. Patent No. 6,407,435 to Ma et al., or, in the alternative, under 35 U.S.C. 103(a) as obvious over Ma et al. in view of Wallace et al.

Regarding claim 3, Ma discloses a semiconductor device (figures 1 and 2) comprising: a semiconductor substrate (112); a gate insulating film (116) provided on the semiconductor substrate (figure 2), at least part of the gate insulating film including a metal oxide film (uppermost instance of layer 140 in figure 2; column 4, lines 37-41). Insofar as the applicant defines the insulating film containing metal, silicon, and oxygen as a film which may contain separated metal oxide and silicon oxide (see page 7 of the specification of the present

application, lines 10-17), Ma is considered to include an insulating laminate film (bottommost instance of 130 and 140) containing metal, silicon, and oxygen (column 4, lines 33-41), provided between the semiconductor substrate and the metal oxide film (figure 2), wherein each of the metal oxide film and the insulating film is an amorphous film (column 2, lines 1-6; column 4, lines 8-18).

Alternatively, assuming arguendo, the silicon nitride/metal oxide laminate films of Ma cannot be considered an insulating film containing metal, silicon, and oxygen.

Wallace discloses a single, graded composition gate insulating film containing metal, silicon, and oxygen (column 2, lines 28-30; lines 45-58).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the silicon oxynitride/metal oxide laminated films of Ma such that they comprise a single insulating film, as taught by Wallace. The rationale is as follows: One of ordinary skill in the art at the time the invention was made would have been motivated to replace the laminate film with a single, graded film, because the structure of the graded film is substantially similar to the laminate film (Wallace, column 6, lines 43-54), but provides the additional benefit of reduced interface state densities due to bonding of discontinuous materials (Wallace, column 2, lines 46-61).

Regarding claim 4, Ma discloses a flat insulating film (311; figures 6-8) having a gate opening portion (300) in which the amorphous metal oxide film (topmost instance of 340) and the gate insulating film containing metal, silicon, and oxygen (bottommost instance of 330 and 340) are formed; and a gate electrode (418) formed on the gate insulating film in the gate opening portion and having a surface which is flush with the flat insulating film (figure 8).

7. Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wallace et al. in view of U.S. Patent No. 6,261,887 to Rodder.

Regarding claim 12, Wallace discloses a semiconductor device comprising: a semiconductor substrate (column 4, lines 14-15); transistor regions having a gate insulating film (36) at least a part of which includes an insulating film containing metal, silicon, and oxygen (column 2, lines 28-30; lines 45-58), where the composition ratios of the metal elements, silicon, and oxygen are the same across the substrate.

Wallace fails to disclose distinct first and second transistor regions wherein the composition ratios in the gate insulating films in the first and second regions are different.

Rodder discloses distinct first and second transistor regions (16 and 18; column 4, lines 19-30), wherein the gate insulating films have different compositions/dielectric constants (column 11, lines 30-60).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the semiconductor device of Wallace, such that first and second transistor regions are provided, where the composition ratios of the gate dielectric are different in the first and second regions, as taught by Rodder. The rationale is as follows: One of ordinary skill in the art at the time the invention was made would have been motivated to provide first and second transistor regions, because for CMOS technology, which is useful for low-dissipation logic circuits, both npn and pnp transistor regions need to be provided and separately optimized (Rodder, column 1, lines 32-44). One further would have been motivated to provide gate insulation layers which differ in concentration between the two regions, because the two regions

need gate layers with different work functions and threshold voltages, and a person skilled in the art would recognize that changing the composition ratios of the material in the two regions would change the dielectric constant, and thus allow for separate optimization of the work function and threshold voltage in each region, without introducing new materials into the fabrication procedure (Rodder, column 11, lines 30-60).

Regarding claim 13, Wallace discloses a semiconductor device comprising: a semiconductor substrate (column 4, lines 14-15); and transistor regions having a gate insulating film (36) at least a part of which includes an insulating film containing metal, silicon, and oxygen (column 2, lines 28-30; lines 45-58), provided across the whole substrate. The insulating film containing metal, silicon, and oxygen is a metal oxide film.

Wallace fails to disclose distinct first and second transistor regions.

Rodder discloses distinct first and second transistor regions (16 and 18; column 4, lines 19-30).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the semiconductor device of Wallace, such that first and second transistor regions are provided, as taught by Rodder. The rationale is as follows: One of ordinary skill in the art at the time the invention was made would have been motivated to provide first and second transistor regions, because for CMOS technology, which is useful for low-dissipation logic circuits, both npn and pnp transistor regions need to be provided and separately optimized (Rodder, column 1, lines 32-44).

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. U.S. Patent No. 6,319,730 to Ramdani et al. discloses a high dielectric constant structure comprising a film of metal, silicon, and oxygen with a second metal oxide film.

b. U.S. Patent No. 6,417,546 to Trivedi et al. discloses a CMOS structure with gate dielectrics varying in nitrogen composition between a first and a second transistor region.

c. U.S. Patent No. 5,876,788 to Bronner et al. discloses a gate dielectric comprising metal, silicon, oxygen, and nitrogen.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Dolan whose telephone number is (703) 305-3233. The examiner can normally be reached on Monday-Friday 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead, Jr. can be reached on (703) 305-4940. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Jennifer M. Dolan
Examiner
Art Unit 2813

Carl Whitehead

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jmd
November 13, 2002